



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,955	08/31/2001	Arulkumar P. Shanmugasundram	5918/04/FPS/MMCS/APC/DV	2623

32588 7590 05/05/2004

APPLIED MATERIALS, INC.
2881 SCOTT BLVD. M/S 2061
SANTA CLARA, CA 95050

EXAMINER

UMEZ ERONINI, LYNETTE T

ART UNIT	PAPER NUMBER
----------	--------------

1765

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/943,955

Applicant(s)

SHANMUGASUNDRAM ET AL.

Examiner

Lynette T. Umez-Eronini

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) 28-33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/18/2003.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-27 in Paper filed 2/5/2004 is acknowledged. The traversal is on the ground(s) that the distinctness of claims drawn to a polishing method in Group I and the claims drawn to a polishing apparatus in Group II was not made cleared; there is no serious burden on the Examiner in examining the inventions of Group I, II, and III; and amending claim 29 and adding linking claim 33, render the restriction improper. This is not found persuasive because it has been shown that the inventions of Group I and II are distinct because the process as claimed can be practiced by another materially different apparatus or by hand, such as one that does not require a carrier assembly having a plurality of arms; it has been shown that Groups I, II, and III are drawn to different inventions and each have different class/subclass, which would be a burden to the examiner to search different inventions; and last, the restriction of the claimed invention was based on the original presentation of the claims, and not the addition of amended claim 33. For the purpose of restriction, claim 33 falls with Group II claims 28 and 29.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Art Unit: 1765

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

On lines 1-2, "wherein the first polishing recipe is determined empirically" is indefinite because its meaning is unclear.

Claim Rejections – 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

Art Unit: 1765

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-3, 5, and 14-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,240,552).

Li teaches a method for chemically mechanically planarizing (CMP) a semiconductor wafer includes directing acoustic waves at the wafer, receiving reflected acoustic wave form the wafer during the cmp process, and analyzing the acoustic waves data and reflected acoustic waves data to determine the thickness of the wafer. The process parameters of the cmp process can then be adjusted as required to improve the uniformity of the process. The parameters include the time, rotational speed, wafer backside pressure down force, and polishing slurry composition (Abstract and column 3. line 53 – column 4, line 48; and column 5, lines 11-65). Li further teaches use a computer (same as applicants' recordable medium) to analyze the wave signals and use this information to develop a thickness map or a similar criteria for evaluating the characteristics of a wafer during the cmp process and adjust the cmp parameters as required (column 6, lines 22 – column 7, line 5). The aforementioned reads on,

A method of producing a uniform wafer thickness in a polishing operation, comprising

Art Unit: 1765

a) providing a model for a wafer polishing that defines a region on a wafer and identifies a wafer material removal rate in a polishing step for the regions; and

(b) polishing a wafer using a polishing recipe that generates a target thickness profile for the region, **in claims 1, 3, 5, and 15-17**;

A method of controlling surface non-uniformity of a wafer in a polishing operation, comprising: a) providing a model for a wafer polishing that defines a region on a wafer and identifies a wafer material removal rate in a polishing step of a polishing process for the region, wherein the polishing process comprises a plurality of polishing steps;

b) polishing a wafer using a first polishing recipe based upon an incoming wafer thickness profile;

c) determining a wafer thickness profile for the post-polished wafer of step (b); and

d) calculating an updated polishing recipe based upon the wafer thickness profile of step (c) and the model of step (a) to maintain a target wafer thickness profile, **in claim 2**; and

A method of determining a model for wafer thickness profile, comprising:

(a) measuring pre-polished wafer thickness in a region defined on one or more wafers;

(b) polishing the one or more wafers, wherein polishing comprises polishing the one or more wafers in a plurality of polishing steps;

(c) measuring the wafer material removal rate for the one or more wafers at each of the plurality of regions after each of the polishing steps of step (b);

Art Unit: 1765

(d) providing a model defining the effect of tool state on polishing effectiveness;
and

(e) recording the pre-polished and post-polished wafer thicknesses for each or the regions on a recordable medium, **in claims 21-24 and 27.**

Li differs in failing to teach providing a model for wafer polishing for a plurality of regions on a wafer, **in claims 1, 2, 14, and 21.**

It would have been obvious to one having ordinary skill in the art of the time of the claimed invention to employ Li's method of polishing a single wafer surface as well as plurality of regions on a wafer as claimed by applicants for the purpose of determining the end point detection during a semiconductor cmp process.

Li further differs in failing to teach the equations as recited **in claims 18-20 and 25-26.**

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use known mathematical methods to formulate and model equations polishing semiconductors for the purpose of fitting experimental data to a real-time process.

8. Claims 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US '552) as applied to claim 1 above.

Li differs in failing to specify the number and type of polishing stations used in the polishing step.

Art Unit: 1765

It would have been obvious to one having ordinary skill in the art of the time of the claimed invention to employ known methods of polishing a wafer in a polishing station as well as in a plurality of polishing stations as claimed by applicants for the purpose of speeding up the step of polishing semiconductor wafers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ltue

May 3, 2004

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

